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Hierarchical Hardware Architecture of Discrete Wavelet Transform For Image Compression

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Abstract: **Recently images comprise a heavy part of future wireless data. Arising mobile devices and wireless sensors require algorithms that get along with the representation of the input data in a proper form for storage and transmission. One approach to diminish this problem is to eliminate redundant information from the transmitted images or frames data over the wireless channel through image compression techniques. However current software performance disregards the time and resources throughout compression and RF wireless transmission. Though, these efforts fall short of meeting real-time processing requirements.In this paper flexible hardware architecture of multi-level decomposition Discrete Wavelet Transform (DWT) has proposed for image compression application. This architecture of DWT decomposition is described and synthesized with VHDL based methodology. The design can be achieved on any targeting FPGA device with slight changes. It facilitates every size of image and any level of decomposition. In order to reduce computational complexities Haar wavelet has been used. The competed size utilization of this 2D DWT multilevel core can be used to counter severe hardware constraints of various wireless and mobile devices applications.**

Keywords: **2D DWT, Linear algebra of DWT, Haar wavelet, VHDL, FPGA.**

I. INTRODUCTION

For future wireless technologies, the most significant challenges will be the requirement to process and transmit a very big volume of image data.The main restrictions in image transmission and storage applications are the memory and bandwidth usage [1]. One approach to relieve this complexity is to reduce the size of transmitted data over the wireless channel using compression techniques. These approaches focus on obtaining higher compression ratio with minimum degradation in the image quality. The most universally used image coding and decoding standard in today's world is Joint Photographic Experts Group (JPEG). However JPEG has many limitations using Discrete Cosine Transform (DCT) kernel, especially at low bit-rate applications [1] [2]. Accordingly to terminate all those limitations and to append new enhanced features. The JPEG2000 is proposed to provide a new image compression system using modern compression techniques, based on the use of wavelet technology.

DWT has traditionally been implemented by convolution method which is the earlier method of finite impulse response (FIR) filter bank structures [3]. A new approach is called the lifting scheme (LS) based on a spatial construction of the wavelet. It is very resilient scheme for its factorization that has been suggested in [4].

The wavelet based image compression performance depends to a large extent on the selection of the wavelet type [5]. The wavelet considered in this paper is the traditional Haar wavelet for simplification. The superior attributes of the Haar transform, including fast and memory efficient, since it can be calculated in place. It is exactly reversible without the edge effects that are a problem with other wavelet transforms. The technical disadvantage of the Haar wavelet is that it is not continuous, and therefore not differentiable. This property can, however, be an advantage for the analysis of signals with sudden transitions [1] [6].

The existing software compression algorithms are not applicable for mobile and wireless communication networks. These algorithms need very complex hardware requirements. Recently, the Field Programmable Gate Array (FPGA) technology presents the potential of designing high achievement systems at low cost. The main objective of this paper is the hardware description of the hierarchical architecture of Haar DWT candidate using FPGA technology [7].

This paper is organized as follows. Section two describes the related architecture implementation of DWT. Section three explains the design of wavelet transform architecture. Section four describes the performance results and the conclusions are made in section five.

II. RELATED WORKS

Several architectures of DWT were proposed combined lossy and lossless transform in the literature. The main goal of the work in [8], is to embed the 5/3 wavelet computation into the 9/7, in order to reduce the number of adders compared to other solutions. In [9] the proposed architecture can be reconfigured for 5/3 and 9/7 wavelet transforms. This reduces significantly the required hardware cost and power consumption of design. The architecture for 1D-DWT principle can be extended to 2D-DWT architectures in [10] is similar to the one developed in [11], [12]. The other based pyramid algorithm was developed in [15] which have the same device of the architecture in [13]. The design presents various transformations like the 1D-DWT, 2D-DWT and multi level decomposition of 5/3 DWT.

In this work, modified 2D-DWT architecture is designed based on Haar transformation technique. The proposed architecture includes reconfigurable transforms modules1D-DWT and 2D-DWT with the multi-levels resolution for the up needs without changing the design. VHDL model for the architecture description is simulated by using Altera Cyclone II 2C35 FPGA device.

Fig. 1: Hardware implementation scheme for the FDWT

III. DESIGN METHODOLOGIES

The scheme involves the collaborative effort of MATLAB toolbox .The different sized images in the grayscale format is originally stored in the PC. It is then stripped of its image header information using the MATLAB program to produce a raw hex file that is ready to be loaded into the embedded bank ram of the FPGA board. Quartus II software used for loading image hex file into FPGA program which produces the resulted wavelet coefficients hex data. This hex file is converted to a grayscale format image file by the MATLAB Program that is used at both input and output stages to inspect the content of the memory files. The 2D-DWT hardware architecture consists of forward DWT (FDWT) and inverse DWT (IDWT) in row-column fashion on the input image text file. Both of these modules is considered as hierarchical scheme that uses separable transforms that can be implemented using one-dimensional filters module on the rows first and then on the columns (or vice versa).

The row filter calculates the DWT of each row of the external memory image data. The column filter calculates the vertical DWT as soon as there are sufficient coefficients generated by the row filter. Then, the resulting decomposed high-pass and low-pass coefficients are stored in intermediate buffers location in external memory.

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The FDWT module in which consist of adder, subtractor and right shifter is used to find out low-pass average and high-pass difference component. First current and next pixel samples are given to the adder then output of adder right shifted by one to give division by two average low-pass wavelet components. The difference component is calculated by subtracting current and next pixel values with shift to right operation. The design implements a comparable code in the IDWT without shift to right operation. Hardware realization procedures for the FDWT and IDWT are depicted in Figure 1 and Figure 2.

Fig. 2: Hardware implementation scheme for the IDWT

The design is composed of three main VHDL modules have been coded to be able to implement this design. The modules are synthesizable two-dimensional DWT module, one dimensional DWT module and external memory unit designed for simulation only as illustrated in Figure 3.

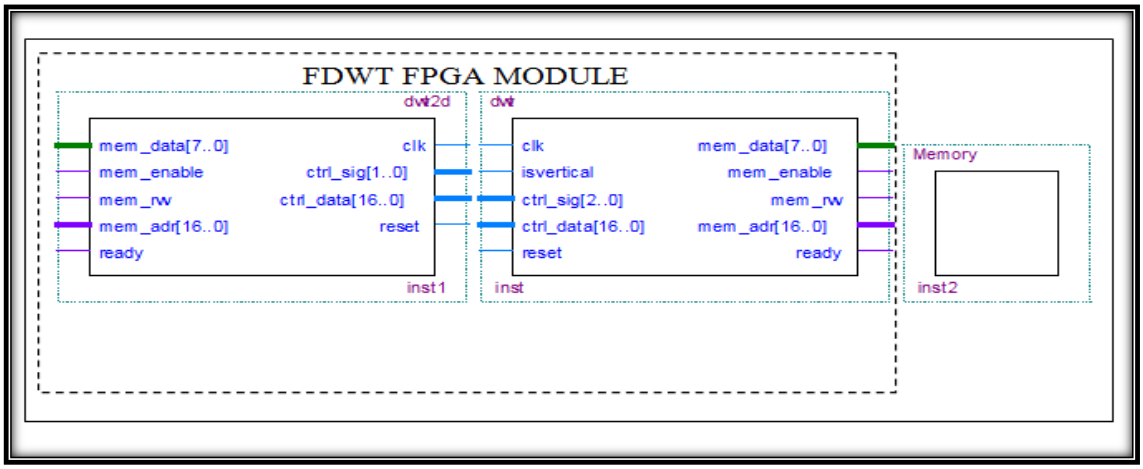

Fig. 3: Block diagram for the proposed hardware architecture for the FDWT

The VHDL coding is done in such a way that the whole code is reusable if the design is to be built-in as sub modules for a larger design. Four adaptation of the design are presented each one adapted different image size. The modules perform 2D-DWT to images of size 64×64, 128×128, 256×256, and512× 512 pixels. These modules can integrate into variety number of transformation levels, from one level to seven levels for entire image compression applications. So while implementing the algorithm in VHDL, linear equations of FDWT and IDWT is used. The Haar equations to calculate an average (L_i) and a wavelet coefficient (H_i) from the current and next pixel samples element in the input image data are computed by Eq(1) and Eq(2), respectively [5]:

$$L(i) = \frac{x(i)+x(i+1)}{2} \qquad (1)$$

$$H(i) = \frac{x(i)-x(i+1)}{2} \qquad (2)$$

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In wavelet terminology the Haar average (L_i) is calculated by the scaling function. The (H_i) coefficient is calculated by the wavelet function. The data input to the forward transform can be perfectly reconstructed using the following 3 and 4 linear algebra equations of IDWT algorithm:

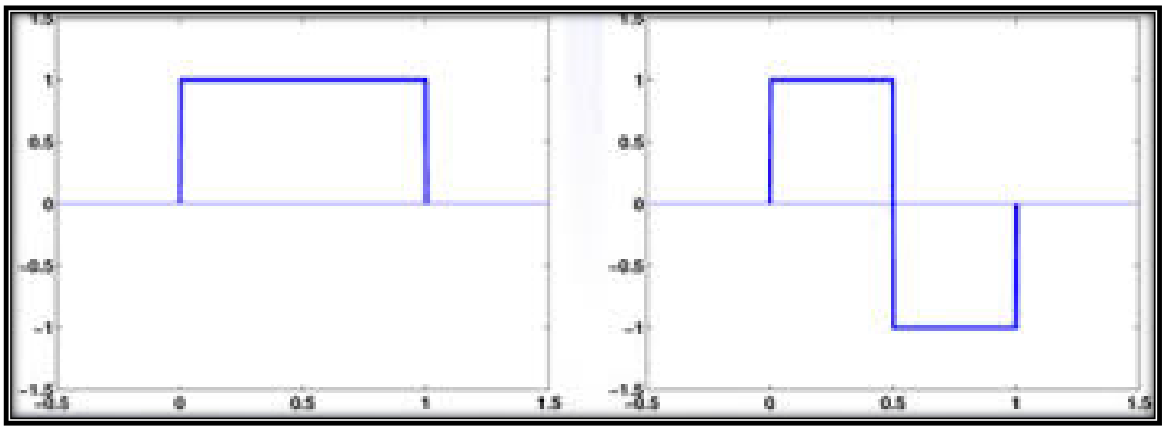
$$x(i) = L(i) + H(i) \quad (3)$$

$$x(i+1) = L(i) - H(i) \quad (4)$$

The 2D-DWT module is collected of 1D-DWT module which represents the central part of the design. The 1D-DWT module computes the wavelet transform coefficients of the input image pixels obtained from the external memory read process. After the computation, the high and low pass coefficients are passed to the memory at the write process. The 2D-DWT module is also responsible for generation of the address for memory reads and writes. For simulation purpose, a memory was modeled using non-synthesizable VHDL code. Memory read and writes processes are use file command which can't be synthesized to internal memory blocks of popular FPGAs. It contains entity that calculates 2-D DWT for image text data and stores results with specified location in external memory, using temporary buffer, also located in external memory. Memory unit needs to be of size twice as the image size, because two chunks of memory are required: one for input image and the other for temporary image data storage.

IV. THE HAAR WAVELET TRANSFORM ARCHITECTURE

The Haar wavelet is the simplest type of wavelet. In discrete form, Haar wavelets are related to a mathematical operation called the Haar transform HT. The Haar transform is an earliest transform from the space domain to a local frequency domain. A HT decomposes each signal into two components, one is called average (approximation) or trend and the other is known as difference (detail) or fluctuation. The Haar transform uses Haar function for its basis as shown in Figure 4.



a- scaling function φ(*t*) **b- wavelet function ψ(*t*)**

Fig. 4 Haar mother wavelet's functions

The Haar wavelet's mother wavelet function ψ(*t*) can be described as a rectangular step function:

$$\psi(t) = \begin{cases} 1 & 0 \le t < 0.5, \\ -1 & 0.5 \le t < 1, \\ 0 & \text{otherwise} \end{cases} \quad (5)$$

And its scaling function φ (*t*) can be described:

$$\varphi(t) = \begin{cases} 1 & 0 \le t < 1, \\ 0 & \text{otherwise} \end{cases} \quad (6)$$

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The Haar wavelet transform is applied iteratively on an image to generate multilevel decomposition. In implementing one-level Haar wavelet transform, a recursive algorithm based on the line based architectures is used as shown in Figure 5.

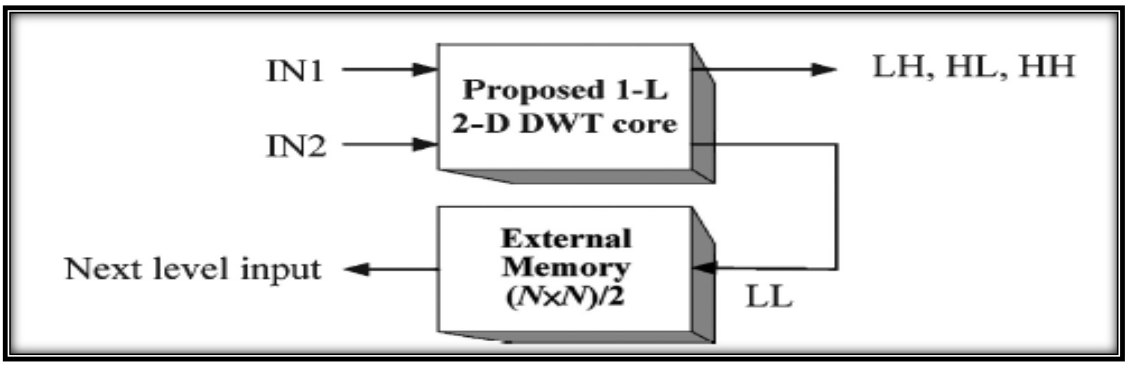

Fig. 5: Block diagram of a one level 2-D DWT.

The image to be transformed is stored in a 2-D array memory. Once all the elements in a row are obtained, the 1D-DWT is performed in that particular row. During the Horizontal Pass process of row-wise 1D-DWT will divide the given image into two parts with the number of rows in each part equal to half that of the image. This matrix is again subjected to a recursive 1D-DWT, but this time column-wise during Vertical Pass process, as depicted in Figure 6.

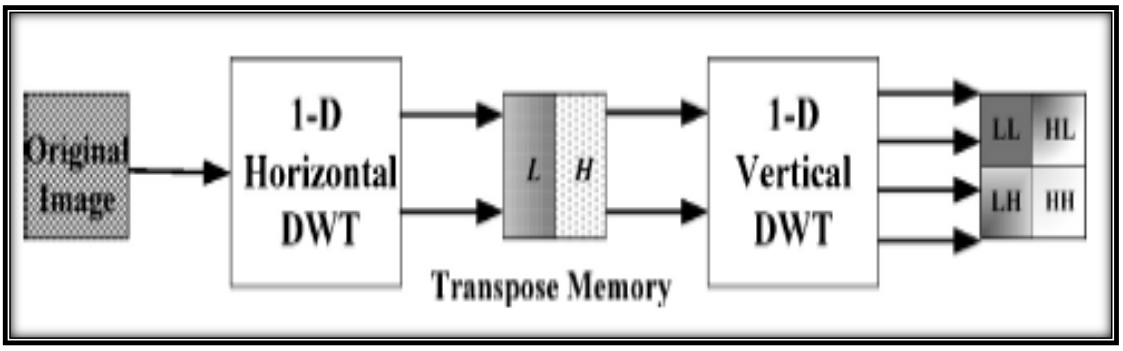

Fig. 6: Diagrammatic flow of a forward 2-D DWT

The four subbands corresponding to the image, with the one obtained by low-pass filtering the rows and columns is referred to as the LL image; the one obtained by low-pass filtering the rows and high-pass filtering the columns is referred to as the LH image; the one obtained by high-pass filtering the rows and low-pass filtering the columns is called the HL image; and the subimage obtained by high-pass filtering the rows and columns is referred to as the HH image, as depicted in Figure 7.

(a) Original imag **(b) 1D Horizontal DWT** **(c) 2D-DWT**

Fig. 7: the four subbands of forward 2-D DWT.

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At level l decomposition, $3l + 1$ sub-bands are produced. A three-level Haar wavelet transform decomposes the original image into ten sub-bands (see Figure 8).

Fig. 8: Three level decomposition for 2D – DWT

V. HARDWARE IMPLEMENTATION RESULTS AND ANALYSIS

Synthesis is performed to transform the VHDL code into logic gate level using Model Sim-Altera 6.5b as shown in Figure 9.

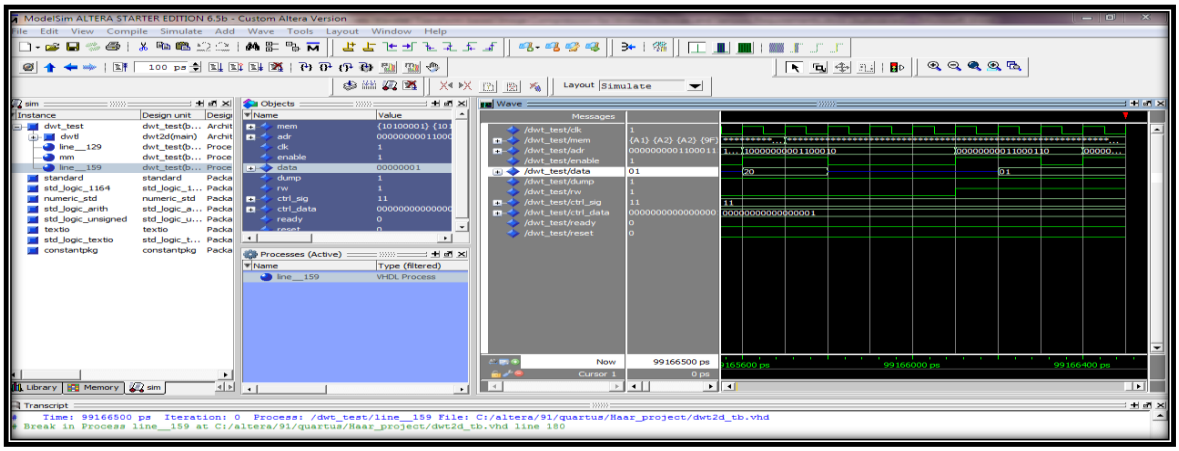

Fig. 9: Model Sim-Altera 6.5b results

The physical hardware layout is generated using (Quartus II 9.1) Web Edition synthesis tools. It is a great design approach to take the VHDL code as a basis and translate it automatically into a net list. After synthesis, RTL views and Technology views have been achieved. One sample Technology view is given in Figure 10. The achieved system period = 20 ns. In term of slices number, ours design requires only 722 slices compared to the 1835 slices for the [13] work, 11765 slices, 4720 slices, 7726 slices, and 2646 slices for the [14] [15] [16] and [17] works respectively.

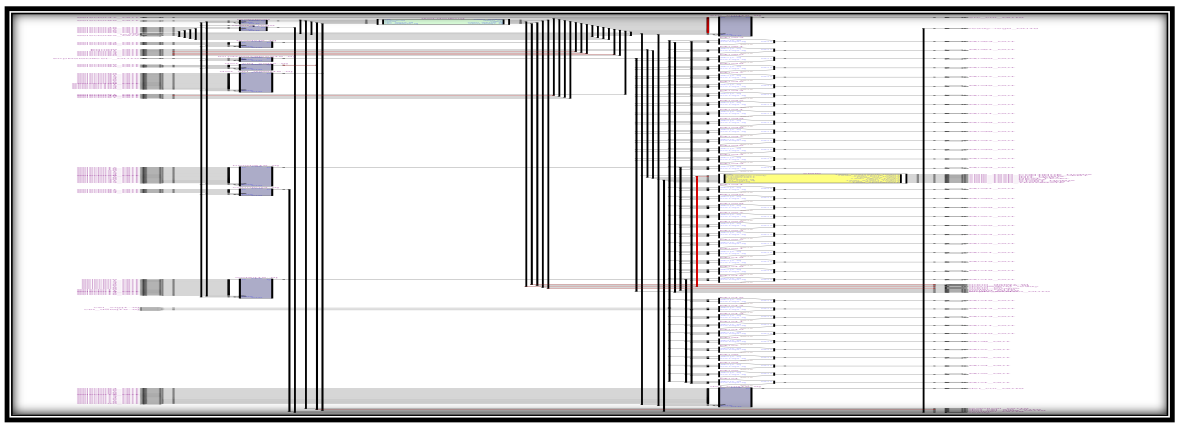

Fig. 10: Register Transfer Level (RTL)

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After simulating the VHDL integrated module in order to extract image we have taken help of MATLAB. Figure 11 shows the final compressed image by using VHDL.

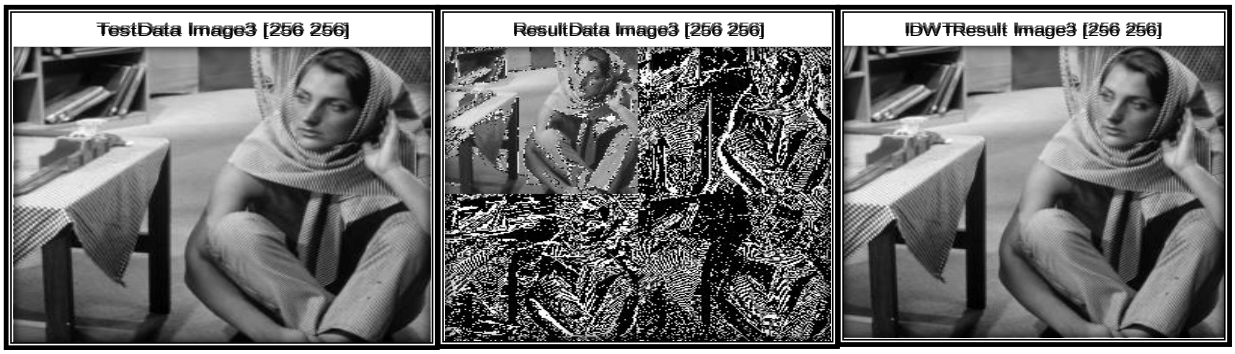

Fig. 11: VHDL code multi-level FDWT results

The inverse wavelet transform of the calculated DWT coefficients, gives a transformed image which will be as same as the original applied image with same number of coefficients. In order to compare these results we will do comparison between Matlab converted test data hex image and IDWT result by using VHDL as shown in Figures 12 and 13.

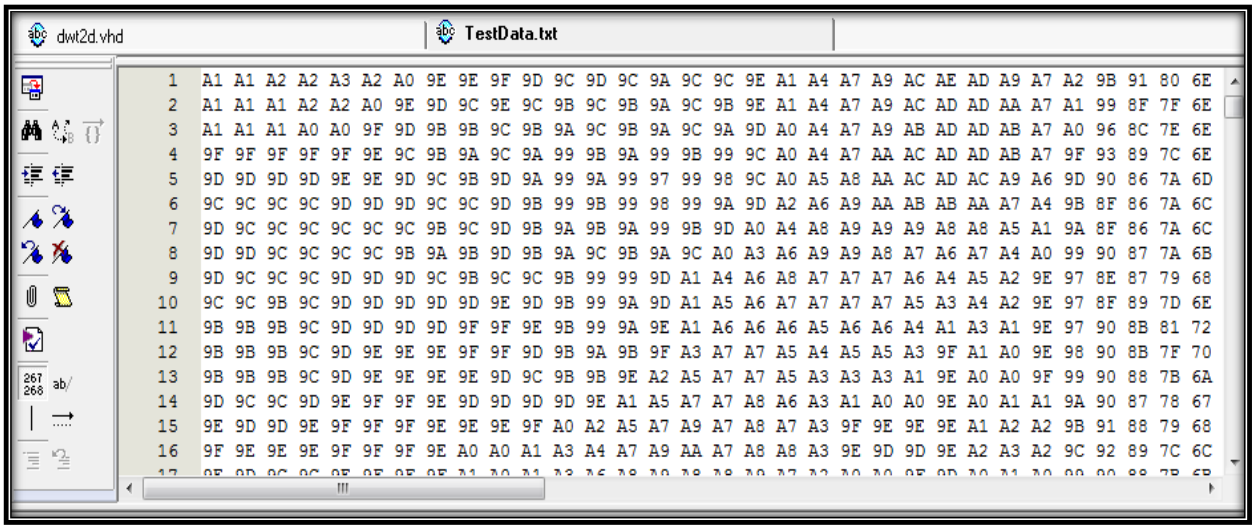

Fig. 12: Results of test hex data of Lena image.

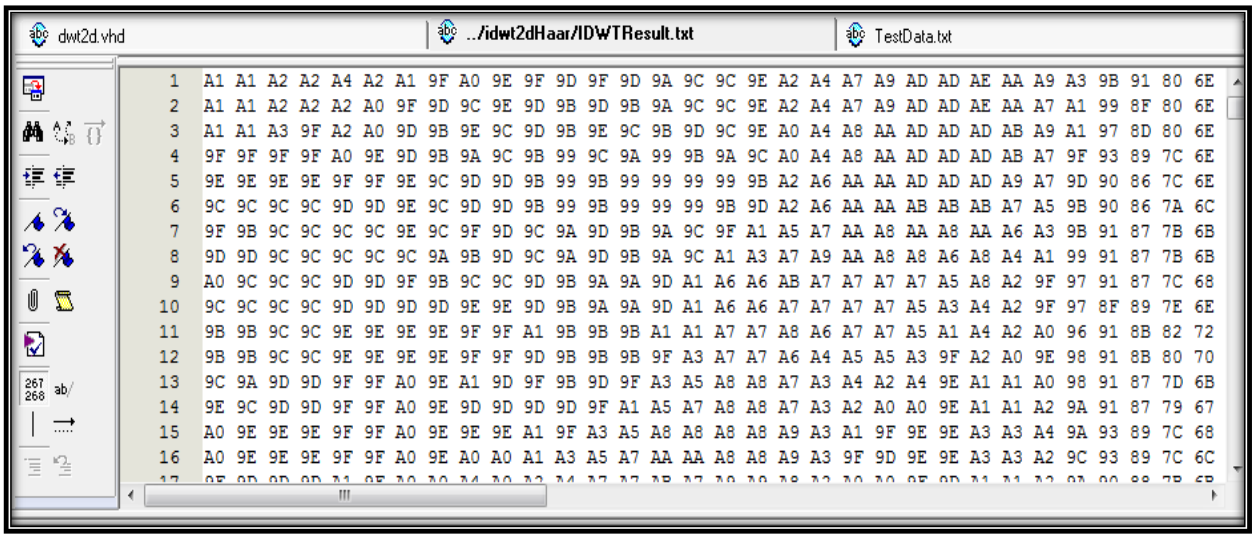

Fig. 13: VHDL program IDWT results of Lena image.

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The number of clock cycles required for various levels of computation starting from the DWT start time until the ready signal is reached. Obviously expanding the number of levels increases the number of clock cycles required for performing the tasks. These tasks include all the necessary computations for the different sized original Lena image as shown in Figures 14 and 15.

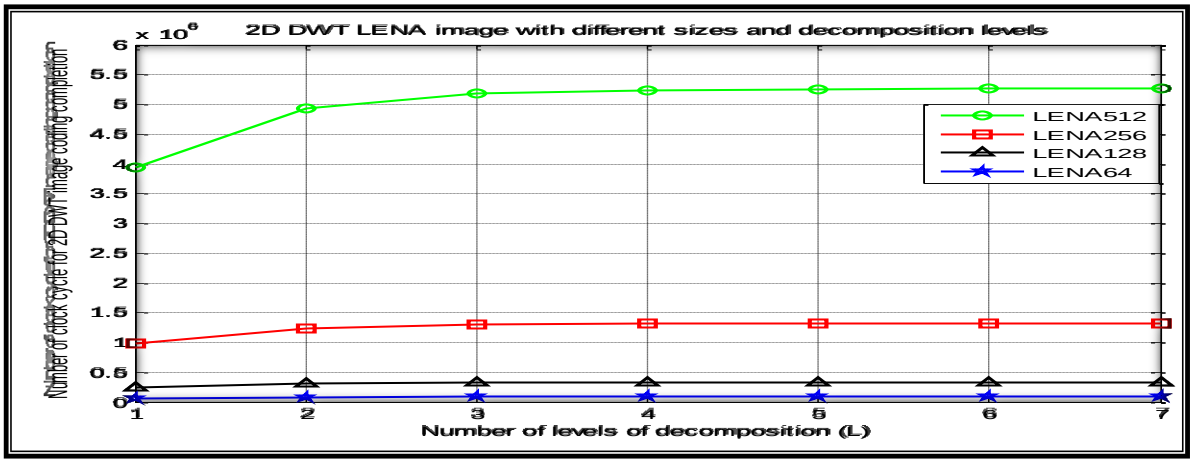

Fig. 14: The number of clock cycles required for FDWT computations tasks

The hardware is designed to be integrated as an extension to custom-computing platform and can be used to accelerate multimedia applications as WSN image transfer.

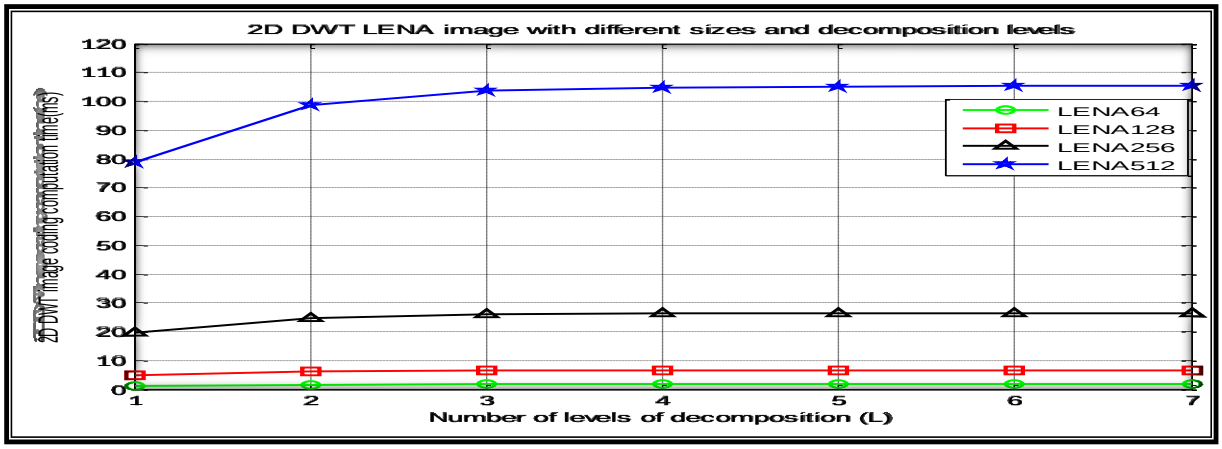

Fig. 15: Computation time required for DWT tasks

Figure 16 shows the difference between software (SW) and hardware (HW) execution time, SW is ten times slower than the HW execution time used in 128×128 pixels of Lena image codec.

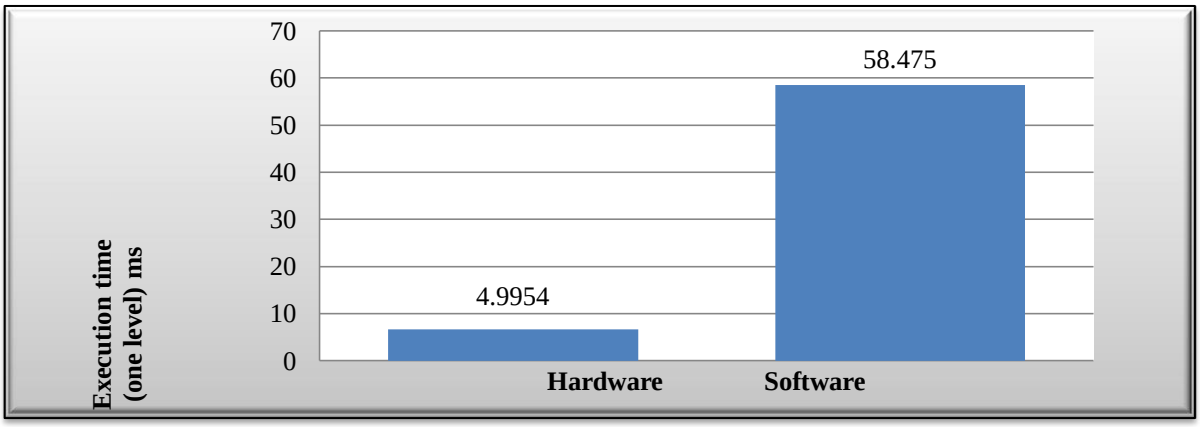

Fig. 16: Computation time required for HW and SW comparison

VI. CONCLUSIONS

This work concentrates on the simple and fast 'Haar' implementation of DWT (FDWT and IDWT) algorithm using VHDL. To reduce the complexity and increase computation speed, linear algebra equations of DWT algorithm are used. The module performs 2D DWT to images of different size pixels. This VHDL code was also synthesized to achieve the gate level architecture of the design which is ready to be executed in hardware environment. Synthesis process showed that the three versions is similar in the maximum frequency and the used slice of the target device, while the difference comes out in the number of clock cycles required for coding. In addition to image size, number of clock cycles is also dependent on the number of levels required. From the satisfactory simulation results we can conclude that algorithm works properly. We have found that higher decomposition is expected to cause higher compression ratio. The feasible physical layout of this design helps the hardware module to implement in many portable and embedded applications. While the changeable level of transformation and its reliable performance makes the design realistic to a wider range of applications such as mobile devices and wireless sensors.

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